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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,435	10/28/2003	Gururaj Pangal	112-0123US	4461

29855 7590 10/20/2006

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EXAMINER	
SUN, SCOTT C	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,435	PANGAL ET AL.	
	Examiner	Art Unit	
	Scott Sun	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/19/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed 7/19/2006, with respect to the double patenting rejection have been fully considered and are persuasive. The double patenting rejection of claims 1, 9, 17, 25 has been withdrawn.

2. Applicant's arguments with respect to the U.S.C 102 rejection have been fully considered but they are not persuasive. Applicant's arguments are summarized as:

a. Regarding claim 17, prior art of record does not teach "port processors" included in an input/output module.

b. Further regarding claim 17, prior art of record teaches neither "snapshotting" nor "journaling".

c. Regarding claim 18, prior art of record does not teach "virtual target task" or "virtual initiator task".

d. Further regarding claim 18, the required elements are not in the input/output module, but instead are in the control module as in the rejection of claim 19.

3. Regarding argument 'a', examiner notes that Edsall teaches (paragraph 53) that "data is received by an intelligent port via a bi-directional connect 302... MAC block 304 is provided, which enables frames of various protocols such as Ethernet or fibre channel to be received... switch 306 determined whether an address specified in an incoming frame pertains to access of a virtual storage location". These functions clearly corresponds to the functionalities of "receive, operate on, and transmit network traffic"

performed by the port processors. Although Edsall does not call these elements "port processors", they clearly have processing capabilities, and they include functionalities that are identical to those claimed by applicant, and are also included in the port of Edsall's virtualization switch. Therefore, the elements 302, 304, 306 can be corresponded to the "port processors" claimed by applicant.

4. Regarding argument 'b', examiner notes that applicant points out that Edsall's journaling and snapshotting are different from what applicant defines and teaches in paragraphs 207-214 and 168-199. However, these paragraphs do not include an explicit definition of the terms, but merely discussions on how to perform these functions. Accordingly, examiner asserts that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

5. Regarding argument 'c', examiner notes that Edsall's invention is directed to a virtualization switch, which Edsall discusses in detail in both the background and throughout the specification. Part of the functionality of a "virtualization switch" is allowing the hosts and storage devices to interact through the virtualization switch. Accordingly, the switch communicates with the storage devices appearing as a host (hence virtual initiator) using physical address of the storage devices and communicates with the hosts as the storage devices (virtual target) using logical (or virtual) address of the storage devices. These terminologies are commonly used with the SCSI protocol to describe the host and device interfaces of the virtualization switch (see background of Edsall, and paragraph 45). Accordingly, "virtual initiator task" and "virtual target task"

are, respectively, the commands used to communicate with the host and devices coupled to virtualization switch.

6. Regarding argument 'd', examiner notes that claims 18 and 19 do not depend on each other, and therefore claim 19 do not include the limitations of claim 18 and vice versa. Furthermore, claim 18 recites "virtual target task" and "virtual initiator task" which are different from the "virtual target" and "virtual initiator" claimed in claim 19. Therefore, the rejections of the two claims are necessarily different. It is uncertain what applicant believes to be the inconsistency in the two claim rejections, and a further clarification of the argument is requested. As noted above in response to argument 'c', the "virtual initiator task" and the "virtual target task" can be the commands used by the input/output module to communication with the host and storage devices connected to the virtualization switch.

7. Having addressed each of applicant's arguments, examiner notes that previous grounds of rejection are still proper, and are attached below with minor changes to better clarify the rejection.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Edsall et al (PG Pub 2003/0172149).

10. Regarding claim 17, Edsall discloses a network (SAN, figure 1B) comprising:

at least one host (hosts 144, 146) adapted to be connected to a switched fabric (switched fabric made up of switches 148, 150, 152; inter-switch links 154, 156; paragraphs 39, 40);

at least two storage units (storage devices 132-142) adapted to be connected to a switched fabric (switches 148, 150, 152; inter-switch links 154, 156);

a switched fabric (switches 148, 150, 152; inter-switch links 154, 156) connected to and coupling the at least one host and the at least two storage units (paragraph 39), the switched fabric comprising:

at least one switch (switches 148, 150, 152) for coupling to the at least one host and the at least two storage units; and

a storage processing device (port processing logic in the switches, shown in figure 3A; paragraph 53) coupled to the at least one switch and for coupling to the at least one host and the at least two storage units, where the host and the at least two storage units may be directly connected to the storage processing device or may be coupled to the storage processing device through the switch, the storage device including:

an input/output module (logic elements 302, 304, 306, 320, 322, 324) including processors to receive, operate on, and transmit network traffic (paragraph 53), and

a control module (virtual processor 308) coupled to said input/output module, said input/output module and said control module being configured to interactively perform virtualization of a storage unit (paragraph 54) and one of snapshotting of data on a storage unit (point in time copying, paragraph 43), journaling of data being written to a storage unit (logging information; paragraph 43), or migrating data between first and second storage units whether the at least one host and the at least two storage units are directly connected to the storage processing device or are coupled through the switch.

11. Regarding claim 18, Edsall discloses the network of claim 17 and further discloses wherein said processors include a processor with a frame classification module (virtualization intercept switch 306), a virtual target task, and a virtual initiator task (commands to host and storage devices). Examiner notes that Edsall teaches performing storage virtualization with the switched fabric (background, paragraph 45). The virtualization switch communicates with the hosts as a target and communicates with the storage devices as an initiator. Accordingly, the commands in the input/output module (elements 302-306) that communicate with the storage devices are virtual initiator tasks; and the commands that communicate with the hosts are virtual target tasks.

12. Regarding claim 19, Edsall discloses the network of claim 17, and further discloses where said input/output module and said control module support a virtualization processor (logic of virtual processor 308 for virtual/physical address mapping) including a virtual target (virtual address of target), a volume manager mapping block (virtual to physical mapping), and a virtual initiator (address of switch; paragraph 54).

13. Regarding claim 20, Edsall discloses the network of claim 19, and further discloses wherein said volume manager mapping block provides virtual block to physical block mappings (paragraph 54).

14. Regarding claim 21, Edsall discloses the network of claim 19, wherein said processors include a processor with a frame classification module, a virtual target task and a virtual initiator task (see rejection for claim 18).

15. Regarding claim 22, Edsall discloses the network of claim 21, wherein said processor utilizes said volume mapping block and said virtual target task to translate received frames from a virtual target to a physical target (paragraph 54).

16. Regarding claim 23, Edsall discloses the network of claim 22, wherein said processor utilizes said virtual initiator task to transmit frames to the physical target and receive response frames from the physical target (paragraph 53, 54; also see rejection for claim 18).

17. Regarding claim 24, Edsall disclose the network of claim 23, wherein the virtual target translates to two physical targets (mirroring; paragraph 64) and whrein said processor utilizes said virtual target task to prepare a command frame for the second

physical target and said virtual initiator to transmit said command frame to the second physical target (paragraph 54).

18. Claims 1-16 and 25-32 are substantially similar to the above claims. The same rejections are applied.

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Sun whose telephone number is (571) 272-2675. The examiner can normally be reached on M-F, 10:30am-7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

KIM HUYNH
SUPERVISORY PATENT EXAMINER

10/16/05